

REMARKS

The Office Action dated April 4, 2005 has been received and the Examiner's comments carefully reviewed. Prior to entry of this paper, Claims 1-20 were pending. Claims 1-5 and 8-20 were rejected, and Claims 6 and 7 were allowed. In this paper, Claims 1, 8, 9, 11, 13, 17, and 20 are amended. Claims 1-20 are currently pending. No new subject matter has been added. For at least the following reasons, Applicant respectfully submits that each of the presently pending claims is in condition for allowance.

Rejection to Claims 1, 3-5, 9, 10, 12, and 17-19

Claim 1 is amended in this paper. The rejection to Claims 1 and 10 are respectfully traversed. It is respectfully submitted that Applicant's Claim 1 as amended is allowable at least because the Nebel does not disclose, "the second shunt circuit is arranged to short the low-range node to the second bias node if a voltage associated with the full-range node corresponds to a logic high", as recited in Applicant's Claim 1 as amended. Also, it is respectfully submitted that Applicant's Claim 10 is allowable at least because Nebel does not disclose, "the first shunt circuit is configured to short the first bias node to the high-range node if the full-range signal corresponds to a logic low", as recited in Applicant's Claim 10.

With regard to Claim 10, the Office Action states, with regard to the circuit illustrated in Fig. 1 of Nebel, "the first shunt circuit (MP21-MP22) is configured to short (connect or conduct) the first bias node (5) from the high-range node (P1) if the full-range signal (IN) corresponds to a logic low (logic 0)." Applicant respectfully disagrees.

In Nebel, node 5 is at the gate of MOSFET MP22, and node P1 is at the gate of MOSFET MP21. In Nebel, when signal IN is a logic 0, MOSFETs MP21 and MP22 are conducting, and operate roughly like closed switches, coupling the drain and source. Since MOSFETs MP21 and MP22 are conducting, the drain and source of MOSFET MP21 are coupled to each other, the drain and source of MOSFET MP22 are coupled to each other, and accordingly the drain of MOSFET MP21 is coupled to the source of MOSFET P22. Accordingly, when signal IN is a logic 0, transistors MP21 and MP22 conduct or connect node PUP to node OUT. However, the gate of MOSFET MP21 (node P1) and the gate of MOSFET MP22 (node 5) are isolated from each other

when signal IN is at logic 0. As is well known in the art, in a MOSFET (such as MOSFETs MP21 and MP22 of Nebel), there is an insulator such as silicon dioxide separating the gate of the MOSFET from the drain and source of the MOSFET, so that substantially no conduction occurs between the gate of the MOSFET and its source or between the gate of the MOSFET and its drain. Accordingly, transistors MP21 and MP22 of Nebel do not connect or conduct node P1 to node N5.

In contrast, Applicant's Claim 10 recites, "the first shunt circuit is configured to short the first bias node to the high-range node if the full-range signal corresponds to a logic low". For at least these reasons, Applicant's Claim 10 is respectfully submitted to be allowable, and notice to that effect is earnestly solicited.

Similarly, in Nebel, when signal IN corresponds to a logic 1, node 6 is not conducted or connected to node N1. In contrast, Applicant's Claim 1 as amended recites, "the second shunt circuit is arranged to short the low-range node to the second bias node if a voltage associated with the full-range node corresponds to a logic high". For at least these reasons, Applicant's Claim 1 as amended is respectfully submitted to be allowable, and notice to that effect is earnestly solicited.

Applicant's Claim 9 is respectfully submitted to be allowable at least for the reasons stated above with regard to Claim 10.

Claims 3-5 and 12 are respectfully submitted to be allowable at least because they depend on Claim 1, which is submitted to be allowable. Claims 17-19 are respectfully submitted to be allowable at least because they depend on Claim 10, which is proposed to be allowable.

Rejection to Claim 2

The rejection to Claim 2 is respectfully traversed. Claim 2 is respectfully submitted to be allowable at least because Nebel does not disclose "the first bias node and the second bias node have approximately the same voltage", as recited in Applicant's Claim 2.

The Office Action states, with regard to the circuit illustrated in Fig. 1 of Nebel, "the first bias node (5) and the second bias node (6) have approximately the same voltage (2.5 Volts)". Applicant respectfully disagrees.

Terminal 5 of Nebel is at 1.4 V, a logic low voltage level sufficient to make PMOSFET MP22 conduct. Terminal 6 is at 3.6V, a logic high voltage level sufficient to make NMOSFET

In contrast, Applicant’s Claim 2 recites, “the first bias node and the second bias node have approximately the same voltage”. For at least these reasons, Applicant respectfully submits that Claim 2 is allowable, and notice to that effect is earnestly solicited.

Claims 8 and 11 have been re-written in independent form. The rejection to Claims 8 and 11 are respectfully traversed.

The Office Action states, “Nebel further teaches the input level transistor circuit of claim 1, wherein the first shunt circuit (MP21-MP22) is configured to influence a resistance between the first bias node (5) and the high-range node (P1) depending on a full-range signal (IN)”. Applicant respectfully disagrees.

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MP21 is Hi Z regardless of the voltage of signal IN. Accordingly, transistor MP21 does not influence a resistance between node 5 and node P1 based on signal IN.

In contrast, Applicant's Claim 8 recites, "the first shunt circuit is configured to influence a resistance between the first bias node and the high-range node depending on a full-range signal". For at least these reasons, it is respectfully submitted that Claim 8 is allowable, and notice to that effect is earnestly solicited. Claim 11 is respectfully submitted to be allowable for reasons analogous to those stated with regard to Claim 8 above.

Rejection to Claims 13-16 and 20

Claims 13 and 20 are not amended for reasons related to patentability, but are amended to comply with the intervening change in case law presented by *SuperGuide Corporation v. DirecTV Enterprises, Inc., et al.*, 358 F.3d 870 (Fed. Cir. 2004).

Applicant respectfully submits that Claim 13 is allowable at least because Nebel does not disclose "ensuring that at least one of: the low-range node is driven during a full cycle of the full-range signal, or the high-range node is driven during the full cycle of the full-range signal", as recited in Applicant's Claim 13.

In Nebel, when signal IN is logic 0, node P1 is floating. Accordingly, node P1 is not driven when signal IN is logic 0.

Similarly, in Nebel, when signal IN is logic 1, node N1 is floating. Accordingly, node N1 is not driven when signal IN is logic 1. In contrast, Applicant's Claim 13 recites, "ensuring that at least one of: the low-range node is driven during a full cycle of the full-range signal, or the high-range node is driven during the full cycle of the full-range signal".

The Office Action states, on page 9, "Regarding claims 13 and 20, the Examiner believes that Nebel inherently teaches the ensuring that at least one of: the low-range node is driven during a full cycle of the full-range signal, and the high-range node is driven during the full cycle of the full-range signal because the structure of Nebel in Fig. 1 is basically the same as the structure of the Applicant in Fig. 2; with the exception of diodes MP11 and MN11." The Office Action further states, "Since the circuit of Nebel in Fig. 1 has the same electrical property of the Applicant's circuit in Fig. 2, Nebel teaches the ensuring that at least one of: the low-range node is driven during a full

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Attachments